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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,489	12/12/2003	James R. Hoff	1000-1349	1864

7590 06/14/2005

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EXAMINER	
LE, DON P	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/735,489	HOFF, JAMES R.
	Examiner	Art Unit
	Don P. Le	2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cartagena (US 6,504,411) in view of Raza et al. (US 6,657,472) and Canaris (US 5,418,473).

3. With respect to claims 1 and 4, figures 1 and 2 of Cartagena disclose an apparatus comprising:

More than one semiconductor register (20a, 20b) logically connected and inputs that are logic gates (31a, 31b). The apparatus of Cartagena dos not specifically disclose the latch as CMOS transistors configured to operate as at least one of a logical cross-coupled NOR Gate SR flip-flop or a logical cross-coupled NAND Gate SR flip-flop and input gates formed by CMOS. Figure 1 of Raza discloses RS flip flop as either logical cross-coupled Nor Gate SR flip-flop or a logical cross-coupled NAND Gate SR flip-flop for the purpose of protecting single event upset. Figures 2 and 3 of Canaris disclose NAND and NOR gates formed by CMOSs for the purpose of protecting single event upset. It would have been obvious to one of ordinary skill of art at the time the invention was made to have implemented the apparatus of Cartagena with the latch formed by either NAND or NOR gates as taught by Raza and the input gates implemented with CMOSs as taught by Canaris for the purpose of preventing single event upset. The apparatus would have the features wherein the CMOS gates are back drive resistant thereby isolating

external circuitry driving the register (this feature is inherent in CMOS circuitry as stated by applicant in the disclosure).

4. With respect to claims 2, 7 and 12, the latch of Cartagena is a memory.

5. With respect to claims 3, 8 and 13, the apparatus of Cartagena overcome radiation effects.

6. With respect to claims 5, 10 and 15, it is given that transistors are driven by input signals.

7. With respect to claims 6, 11 and 14, the combination Cartagena in view of Raza and Canaris disclose a redundant single event upset suppression system, comprising:

at least two semiconductor registers (20a, 20b) logically connected and each including CMOS transistors adapted to operate as a logical cross-coupled Nor Gate SR flip-flop or NAND gate (Raza discloses NOR FF and NAND FF, and Canaris discloses CMOS NOR gate); and

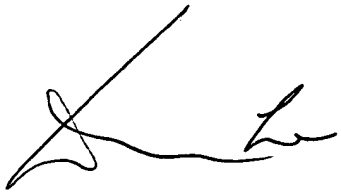
inputs (31a, 31b) to the register comprised of CMOS gates (Canaris discloses CMOS gates) acting as insulators (inherent as discloses by applicant).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don P. Le whose telephone number is 571-272-1806. The examiner can normally be reached on 7AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

6/10/2005



DON LE
PRIMARY EXAMINER